EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	132	(Murayama near Hideki).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L2	247	(Horikawa near Kazuo).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L3	84	(Yashiro near Hiroshi).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L4	44	(Yamauchi near Masahiko).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L5	542	(Ishii near Yasuhiro).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L6	29	(Sasaki near Daisuke).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L7	21704	memory adj2 size	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L8	136564	(EPROM or EEPROM or FLASH or nonvolatile) adj2 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L9	1518	hot adj2 insert$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44

EAST Search History

L10	17438	size adj2 information	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L11	7647	memory adj2 allocation	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L12	378	expandable adj2 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L13	1204329	bank or module or segment	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L14	10796	(virtual or logical) near2 map$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L15	5123	DLAT or TLB	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:44
L16	168218	initializ$4 or ((raw or cold) adj boot)\	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:48
L17	970	1 or 2 or 3 or 4 or 5 or 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:48
L18	4246	7 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:49
L19	18690	address near3 translat$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:49

EAST Search History

L20	19	9 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:50
L21	5	18 and 20	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:50
L22	18	11 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:50
L23	2	22 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:50
L24	0	21 and 23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:50
L25	4	21 and 19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:50
L26	0	25 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/07 12:50

Terms used
hot insert hot plugged virtual or **logical physical address translation**

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1 Level set and PDE methods for computer graphics

David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker
August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**
Publisher: ACM Press
Full text available: pdf(17.07 MB) Additional Information: full citation, abstract

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

2 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren
November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**
Publisher: IBM Press
Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

3 PIROL: a case study for multidimensional separation of concerns in software engineering environments

Stephan Herrmann, Mira Mezini
October 2000 **ACM SIGPLAN Notices , Proceedings of the 15th ACM SIGPLAN conference on Object-oriented programming, systems, languages, and applications OOPSLA '00**, Volume 35 Issue 10
Publisher: ACM Press
Full text available: pdf(441.79 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present our experience with applying multidimensional separation of concerns to a software engineering environment. By comparing two different designs of our system, we show the importance of separating integration issues from the implementation of the individual concerns. We present a model in which integration issues are encapsulated into rst--class connector objects and indicate how this facilitates the understandability, maintenance and evolution of the system. We identify ...

Keywords: component integration, domain—specific language, separation of concerns, software engineering environment

4 The elements of nature: interactive and realistic techniques

Oliver Deusen, David S. Ebert, Ron Fedkiw, F. Kenton Musgrave, Przemyslaw Prusinkiewicz, Doug Roble, Jos Stam, Jerry Tessendorf

August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**

Publisher: ACM Press

Full text available: pdf(17.65 MB) Additional Information: full citation, abstract

This updated course on simulating natural phenomena will cover the latest research and production techniques for simulating most of the elements of nature. The presenters will provide movie production, interactive simulation, and research perspectives on the difficult task of photorealistic modeling, rendering, and animation of natural phenomena. The course offers a nice balance of the latest interactive graphics hardware-based simulation techniques and the latest physics-based simulation techni ...

5 Pen computing: a technology overview and a vision

André Meyer

July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3

Publisher: ACM Press

Full text available: pdf(5.14 MB) Additional Information: full citation, abstract, citings, index terms

This work gives an overview of a new technology that is attracting growing interest in public as well as in the computer industry itself. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar pen and paper interface metaphor. From this follows a set of consequences that will be analyzed and put into context with other emerging technologies and visions.Starting with a short historic ...

6 Link and channel measurement: A simple mechanism for capturing and replaying wireless channels

Glenn Judd, Peter Steenkiste

August 2005 **Proceeding of the 2005 ACM SIGCOMM workshop on Experimental approaches to wireless network design and analysis E-WIND '05**

Publisher: ACM Press

Full text available: pdf(6.06 MB) Additional Information: full citation, abstract, references, index terms

Physical layer wireless network emulation has the potential to be a powerful experimental tool. An important challenge in physical emulation, and traditional simulation, is to accurately model the wireless channel. In this paper we examine the possibility of using on-card signal strength measurements to capture wireless channel traces. A key advantage of this approach is the simplicity and ubiquity with which these measurements can be obtained since virtually all wireless devices provide the req ...

Keywords: channel capture, emulation, wireless

7 Cool-Mem: combining statically speculative memory accessing with selective address translation for energy efficiency

Raksit Ashok, Saurabh Chheda, Csaba Andras Moritz

October 2002 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News , Proceedings of the 10th international conference on Architectural support for programming languages and operating systems ASPLOS-X**, Volume 36 , 37 , 30 Issue 5 , 10 , 5

Publisher: ACM Press

Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, references, citings

This paper presents Cool-Mem, a family of memory system architectures that integrate conventional memory system mechanisms, energy-aware address translation, and compiler-enabled cache disambiguation techniques, to reduce energy consumption in general purpose architectures. It combines statically speculative cache access modes, a dynamic CAM based Tag-Cache used as backup for statically mispredicted accesses, various conventional multi-level associative cache organizations, embedded protection c ...

8 Software controlled memory systems: Energy-efficient address translation for virtual memory support in low-power and real-time embedded processors

Xiangrong Zhou, Peter Petrov

September 2005 **Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis CODES+ISSS '05**

Publisher: ACM Press

Full text available: pdf(150.88 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present an application-driven address translation scheme for low-power and real-time embedded processors with virtual memory support. The power inefficiency and nondeterministic execution times of address-translation mechanisms have been major barriers in adopting and utilizing the benefits of virtual memory in embedded processors with low-power and real-time constraints. To address this problem, we propose a novel, *Customizable Translation Table (CTT)* organization, where ...

9 The state of the art in distributed query processing

Donald Kossmann

December 2000 **ACM Computing Surveys (CSUR)**, Volume 32 Issue 4

Publisher: ACM Press

Full text available: pdf(455.39 KB) Additional Information: full citation, abstract, references, citings, index terms

Distributed data processing is becoming a reality. Businesses want to do it for many reasons, and they often must do it in order to stay competitive. While much of the infrastructure for distributed data processing is already there (e.g., modern network technology), a number of issues make distributed data processing still a complex undertaking: (1) distributed systems can become very large, involving thousands of heterogeneous sites including PCs and mainframe server machines; (2) the stat ...

Keywords: caching, client-server databases, database application systems, dissemination-based information systems, economic models for query processing, middleware, multitier architectures, query execution, query optimization, replication, wrappers

10 GPGPU: general purpose computation on graphics hardware

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn

August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH**

'04

Publisher: ACM Press

Full text available: pdf(63.03 MB) Additional Information: full citation, abstract

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

11 Novel self-test methods: A scalable software-based self-test methodology for programmable processors

Li Chen, Srivaths Ravi, Anand Raghunathan, Sujit Dey

June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(107.71 KB) Additional Information: full citation, abstract, references, index terms

Software-based self-test (SBST) is an emerging approach to address the challenges of high-quality, at-speed test for complex programmable processors and systems-on chips (SoCs) that contain them. While early work on SBST has proposed several promising ideas, many challenges remain in applying SBST to realistic embedded processors. We propose a systematic scalable methodology for SBST that automates several key steps. The proposed methodology consists of (i) identifying test program templates tha ...

Keywords: at-speed test, manufacturing test, microprocessor, scalability, software-based self-test, test program

12 MIL primitives for querying a fragmented world

Peter A. Boncz, Martin L. Kersten

October 1999 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 8 Issue 2

Publisher: Springer-Verlag New York, Inc.

Full text available: pdf(261.36 KB) Additional Information: full citation, abstract, citings, index terms

In query-intensive database application areas, like decision support and data mining, systems that use vertical fragmentation have a significant performance advantage. In order to support relational or object oriented applications on top of such a fragmented data model, a flexible yet powerful intermediate language is needed. This problem has been successfully tackled in Monet, a modern extensible database kernel developed by our group. We focus on the design choices made in the Monet interprete ...

Keywords: Database systems, Main-memory techniques, Query languages, Query optimization, Vertical fragmentation

13 Query evaluation techniques for large databases

Goetz Graefe

June 1993 **ACM Computing Surveys (CSUR)**, Volume 25 Issue 2

Publisher: ACM Press

Full text available: pdf(9.37 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Database management systems will continue to manage large data volumes. Thus, efficient algorithms for accessing and manipulating large sets and sequences will be required to provide acceptable performance. The advent of object-oriented and extensible

database systems will not solve this problem. On the contrary, modern data models exacerbate the problem: In order to manipulate large sets of complex objects as efficiently as today's database systems manipulate simple records, query-processi ...

Keywords: complex query evaluation plans, dynamic query evaluation plans, extensible database systems, iterators, object-oriented database systems, operator model of parallelization, parallel algorithms, relational database systems, set-matching algorithms, sort-hash duality

14 Algorithms and data structures for flash memories

Eran Gal, Sivan Toledo
June 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 2
Publisher: ACM Press
Full text available: pdf(343.39 KB) Additional Information: full citation, abstract, references, index terms

Flash memory is a type of electrically-erasable programmable read-only memory (EEPROM). Because flash memories are nonvolatile and relatively dense, they are now used to store files and other persistent objects in handheld computers, mobile phones, digital cameras, portable music players, and many other computer systems in which magnetic disks are inappropriate. Flash, like earlier EEPROM devices, suffers from two limitations. First, bits can only be cleared by erasing a large block of memory. S ...

Keywords: EEPROM memory, Flash memory, wear leveling

15 A rapid prototyping software infrastructure for user interfaces in ubiquitous augmented reality

Christian Sandor, Gudrun Klinker
May 2005 **Personal and Ubiquitous Computing**, Volume 9 Issue 3
Publisher: Springer-Verlag
Full text available: pdf(725.90 KB) Additional Information: full citation, abstract

Recent user interface concepts, such as multimedia, multimodal, wearable, ubiquitous, tangible, or augmented-reality-based (AR) interfaces, each cover different approaches that are all needed to support complex human–computer interaction. Increasingly, an overarching approach towards building what we call ubiquitous augmented reality (UAR) user interfaces that include all of the just mentioned concepts will be required. To this end, we present a user interface architecture that can form a ...

Keywords: Augmented reality, Frameworks, Mobile systems, Multimodality, Software architectures, Tangible user interfaces, Ubiquitous computing

16 Avoiding conflict misses dynamically in large direct-mapped caches

Brian N. Bershad, Dennis Lee, Theodore H. Romer, J. Bradley Chen
November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the sixth international conference on Architectural support for programming languages and operating systems ASPLOS-VI**, Volume 29 , 28 Issue 11 , 5
Publisher: ACM Press
Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a method for improving the performance of a large direct-mapped cache by reducing the number of conflict misses. Our solution consists of two components: an inexpensive hardware device called a Cache Miss Lookaside (CML) buffer that detects

conflicts by recording and summarizing a history of cache misses, and a software policy within the operating system's virtual memory system that removes conflicts by dynamically remapping pages whenever large numbers of conflict miss ...

17 Microarchitecture-level power analysis and optimization techniques: Energy-effcient physically tagged caches for embedded processors with virtual memory

Peter Petrov, Daniel Tracy, Alex Orailoglu
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(891.39 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present a low-power tag organization for physically tagged caches in embedded processors with virtual memory support. An exceedingly small subset of tag bits is identified for each application hot-spot so that only these tag bits are used for cache access with no performance sacrifce as they provide complete address resolution. The minimal subset of physical tag bits, i.e. the compressed tag, is dynamically updated following the changes in the physical address space of the appli ...

18 Dynamic translation: Dynamic binary translation for accumulator-oriented architectures

Ho-Seop Kim, James E. Smith
March 2003 **Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization CGO '03**
Publisher: IEEE Computer Society
Full text available: pdf(1.13 MB) Additional Information: full citation, abstract, references, citings, index terms

A dynamic binary translation system for a co-designed virtual machine is described and evaluated. The underlying hardware directly executes an accumulator-oriented instruction set that exposes instruction dependence chains (strands) to a distributed microarchitecture containing a simple instruction pipeline. To support conventional program binaries, a source instruction set (Alpha in our study) is dynamically translated to the target accumulator instruction set. The binary translator identifies ...

19 Supervisory and Monitor Systems

Robert F. Rosin
March 1969 **ACM Computing Surveys (CSUR)**, Volume 1 Issue 1
Publisher: ACM Press
Full text available: pdf(1.33 MB) Additional Information: full citation, references, citings, index terms

20 Binary translation and architecture convergence issues for IBM system/390

Michael Gschwind, Kemal Ebcioğlu, Erik Altman, Sumedh Sathaye
May 2000 **Proceedings of the 14th international conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, index terms

We describe the design issues in an implementation of the ESA/390 architecture based on binary translation to a very long instruction word (VLIW) processor. During binary translation, complex ESA/390 instructions are decomposed into instruction "primitives" which are then scheduled onto a wide-issue machine. The aim is to achieve high instruction level parallelism due to the increased scheduling and optimization opportunities which can be exploited by binary translation software ...

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1 ACM Transactions on Algorithms (TALG)
October 2005 periodical
Publisher: ACM Press
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2 ACM Transactions on Sensor Networks (TOSN)
November 2005 periodical
Publisher: ACM Press
Additional Information: full citation

3 ACM SIGITE Newsletter
June 2005 periodical
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4 ACM Journal on Emerging Technologies in Computing Systems (JETC)
July 2005 periodical
Publisher: ACM Press
Additional Information: full citation

5 ACM Transactions on Multimedia Computing, Communications, and Applications (TOMCCAP)
August 2005 periodical
Publisher: ACM Press
Additional Information: full citation

ACM Transactions on Storage (TOS)

6 August 2005 periodical
Publisher: ACM Press
Additional Information: full citation

7 ACM SIGLASH Newsletter
March 1981 periodical
Publisher: ACM Press
Additional Information: full citation

8 ACM Transactions on Speech and Language Processing (TSLP)
February 2005 periodical
Publisher: ACM Press
Additional Information: full citation

9 ACM SIGACCESS Accessibility and Computing
September 2005 periodical
Publisher: ACM Press
Additional Information: full citation

10 IEEE/ACM Transactions on Computational Biology and Bioinformatics (TCBB)
October 2005 periodical
Publisher: IEEE Computer Society Press
Additional Information: full citation

11 ACM SIGMINI Newsletter
August 1978 periodical
Publisher: ACM Press
Additional Information: full citation

12 ACM SIGPC Notes
September 1982 periodical
Publisher: ACM Press
Additional Information: full citation

13 ACM SIGSMALL Newsletter
October 1981 periodical
Publisher: ACM Press
Additional Information: full citation

14 ACM SIGSOC Bulletin
April 1982 periodical
Publisher: ACM Press
Additional Information: full citation

15 ACM Transactions on Applied Perception (TAP)
October 2005 periodical
Publisher: ACM Press
Additional Information: full citation

16 ACM Transactions on Architecture and Code Optimization (TACO)
September 2005 periodical
Publisher: ACM Press
Additional Information: full citation

17 ACM SIGOA Newsletter
April 1986 periodical
Publisher: ACM Press
Additional Information: full citation

18 Computers in Entertainment (CIE)
October 2005 periodical
Publisher: ACM Press
Additional Information: full citation

19 ACM SIGARCH Computer Architecture News
June 2005 periodical
Publisher: ACM Press
Additional Information: full citation

20 Queue
November 2005 periodical
Publisher: ACM Press
Additional Information: full citation

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